## QUESTION BANK WITH 2 MARKS ANSWER

PERIOD: MARCH 2024 - JUNE 2024
BRANCH: CSE
SUB CODE/NAME: BE3251/ Basic Electrical and Electronics Engineering

## UNIT-III ANALOG ELECTRONICS <br> PART A

1. Define Knee Voltage or Junction Barrier Voltage for PN Junction diode? (N/D 2023) In the forward characteristics of a diode once the voltage is applied then the junction starts increasing rapidly. This barrier voltage at which the flow of current will increase is known as Knee Voltage or Junction Barrier Voltage for PN Junction diode.
2. List the applications of IGBTs. (N/D 2023)

It is used in switching power supplies in high power applications:

- Variable frequency drivers (VFDs)
- Uninterruptible power supply (UPS)
- Electric Cars
- Variable Speed Refrigerators
- Air Conditioners

3. List the Applications of Zener diode? (April/May 2023) (Nov/Dec 2015)

- Used as a constant voltage source.
- Used as voltage regulator.

4. Define Latching and Holding Current of SCR? (April/May 2023)

Latching current is associated with the turn on process of SCR. It is the minimum value of anode current which it must attain during the turn on process to maintain conduction when gate pulse is removed.
In a SCRs, holding current is associated with turn-off + process and latching current with the turn-on process.
5. Name the Four operating regions of transistor. (April/May 2022)

Active region: It is defined in which transistor collector junction is biased in reverse direction and emitter junction in forward direction.
Cutoff region: The region in which the collector and emitter junctions are both reversebiased

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Saturation region: The region in which both the collector and emitter junctions are forward biased.

Inverse active region: This region lies between saturation and cutoff. The transistor operates in active region when the emitter junction is forward biased and collector junction is reverse biased. In the active state, collector current is $\beta$ times the base current,
6. Differentiate the operation of rectifiers and inverters? (April/May 2022)

| S. <br> No | RECTIFIERS | INVERTERS |
| :---: | :--- | :--- |
| 1 | A rectifier changes current from <br> alternating current (AC) to direct <br> current (DC) | while an inverter converts DC to AC. |
| 2 | Rectifiers come in two basic types: <br> half-wave and full-wave | Inverter come in two basic types: <br> Single phase inverter an Three phase <br> inverter |

7. Define Semiconductors. (April/May 2022)

Semiconductors are materials having conducting properties lies between conductors and insulators. These materials are separated by a small energy gap (=1ev).Germanium and Silicon are commonly used semiconductors.
8. Draw the circuit of Zener voltage regulator? (Nov/Dec 2022)


Zender diode as a voltage regulator
9. JFET is a voltage operated device. Justify? (Nov/Dec 2022)

A JFET is a voltage-controlled device because the current between the drain and the source is controlled by the voltage at the gate with reference to the source (vgs).

## 10. Define: valence band, conduction band.

The range of energies possessed by valence electrons is called valence band. The range of energies possessed by conduction electrons is called conduction band. The free electrons which are left in the valence band are occupying the conduction band.

## 11. Define: forbidden energy gap

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The energy gap between the valence band and conduction band is defined as forbidden energy gap. For insulators. It is around 6ev, for semiconductors, its value is comparatively low. Germanium has energy gap 0.7 eV and silicon has 1.1 eV . For conductors, since conduction and valence bands are overlapping the energy gap is zero.

## 12. What is intrinsic semiconductor?

Intrinsic semiconductors are pure form of semiconductors. The conductivity of a semiconductor lies between an insulator and a conductor. As temperature increases, the conductivity of the semiconductor also increases. Semiconductors have negative temperature co-efficient of resistance.

## 13. Explain the significance of Base width modulation (Early effect)

It reduces the charges recombination of electrons with holes in the base region; hence the current gain increases with the increase in collector -base voltage. The charge gradient is increased within base hence the current due to minority carriers injected across emitter junction increases.
14. What are the three types of transistor configuration? Among those which is most important?
Common base configuration, Common emitter configuration, Common collector configuration are the three types of transistor configuration. The CE configuration is important because it has high current gain and its Output to input impedance ratio is moderate therefore easy coupling is possible between various transistor stages. It finds excellent usage in audio frequency applications hence used in receivers and transmitters.

## 15. How a transistor is used as a switch?

A transistor should be operated in saturation and cutoff regions to use it as a switch. While operating in saturation region, transistor carry heavy current hence considered as ON state. In cutoff it doesn't carry current and it is equivalent to open.

## 16. Which configuration is known as emitter follower and why it is named so?

CC configuration is known as emitter follower, whatever may be the signal applied at the input, may produce same signal at the output. In other words, the gain of the circuit is unity. So that the common circuit the so called emitter follower is named as emitter follower (output follows the input).
17. Compare the performance of $\mathrm{CE}, \mathrm{CB}, \mathrm{CC}$

| Parameters | CB | CE | CC |
| :--- | :--- | :--- | :--- |
| Current gain $\left(\mathrm{A}_{\mathrm{i}}\right)$ | Low | High | High |

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| Voltage gain $\left(\mathrm{V}_{\mathrm{i}}\right)$ | High | High | Low |
| :--- | :--- | :--- | :--- |
| Input resistance $\left(\mathrm{R}_{\mathrm{i}}\right)$ | Low | Medium | High |

18. What is Zener breakdown? (Nov 2015)

When a PN junction is heavily doped the depletion region is very narrow. So under reverse bias condition, the electric field across the depletion layer is very intense. Electric field is voltage per distance and due to narrow depletion region and high reverse voltage, it is intense. Such an intense field is enough to pull the electrons out of the valence bands of the stable atoms. So this is not due to the collision of carriers with atoms. Such a creation of free electrons is called Zener effect which is different that the avalanche effect. These minority carriers constitute very large current and mechanism is called Zener Breakdown.

## 19. Define load regulation and line regulation

Line Regulation: Ratio of change in output voltage for a corresponding change in the input Voltage expressed as a percentage.
Load Regulation: Ratio of change in the output voltage for a certain range of load current Values, expressed as a percentage.
20. Define Rectifier:

It is an electronic circuit which converts AC input to pulsating DC. i.e., output of the rectifier is not a pure DC. Normally PN diode is used as rectifying device.

## 21. Define PIV of a rectifier with an example.

This is the maximum reverse voltage with which a diode can withstand without any damage. PIV of half wave rectifier is $V_{m}$, while that of center tapped FWR is $2 V_{m}$.
22. Compare the performance analysis of HWR,FWR(Centre tapped) \& bridge rectifier

| Performance factors | HWR | FWR <br> (Bridge) | FWR(Center <br> tapped) |
| :--- | :--- | :--- | :--- |
| Average current | $\mathrm{I}_{\mathrm{m}} / \pi$ | $2 \mathrm{I}_{\mathrm{m}} / \pi$ | $2 \mathrm{I}_{\mathrm{m}} / \pi$ |
| Average dc voltage | $\mathrm{E}_{\mathrm{m}} / \pi$ | $2 \mathrm{~V}_{\mathrm{m}} / \pi$ | $2 \mathrm{~V}_{\mathrm{m}} / \pi$ |
| rms load current | $\mathrm{I}_{\mathrm{m}} / 2$ | $\mathrm{I}_{\mathrm{m}} / \sqrt{ } 2$ | $\mathrm{I}_{\mathrm{m}} / \sqrt{ } 2$ |
| Efficiency | 0.406 | 0.812 | 0.812 |
| TUF | 0.287 | 0.812 | 0.693 |
| Ripple factor | 1.21 | 0.48 | 0.48 |
| PIV | $\mathrm{V}_{\mathrm{m}}$ | $\mathrm{V}_{\mathrm{m}}$ | $2 \mathrm{~V}_{\mathrm{m}}$ |

23. Write any two salient points on a p-n junction. (May 2013)

A junction is formed between a sample of ' P ' type semiconductor and a sample of ' N ' type semiconductor joined together then this device is called the PN junction.
The formation of PN junction is also called as Diode, because it has two electrodes and for P region named as Anode and the other for ' N ' region named as Cathode.
24. When should a transistor be biased? Name two common biasing circuits. (May 2013)

For proper operation of transistor, input junction should be forward biased and the output junction should be reverse biased.
Common base and common emitter configuration are the two common biasing circuits.
25. What is doping? (May 2014)

Doping means adding an impurity to pure semiconductor to impure its electrical conductivity.
26. Give the other names of depletion region. (May 2014)
*Potential barrier region.
*Space charge region or charge free region.
27. What is cut in voltage?

The forward voltage at which the current through the junction starts increasing rapidly is called knee voltage or cut in voltage.
28. Draw the characteristics of Zener diode. (May 2015).

29. Find the values of $I_{C}, I_{B}, \beta$. Transistor values are $\alpha=0.95, I_{E}=1 \mathrm{~mA}$. (May 2015).
$\mathrm{I}_{\mathrm{C}}=\alpha . \mathrm{I}_{\mathrm{E}}=0.95 * 1 \mathrm{~mA}=0.95 \mathrm{~mA}$
$\beta=\alpha /(1-\alpha)=0.95 /(1-0.95)=19$.
$\mathrm{I}_{\mathrm{B}}=\mathrm{I}_{\mathrm{C}} / \beta=0.05 / 19=0.05 \mathrm{~mA}$
30. List various hybrid parameters of transistor. (May 2016).

Voltage gain, input resistance, output resistance, output conductance and current gain.
PART-B \& C

1. Explain the Constructional details and different modes of operation of MOSFET (13 Marks) (A/M 2022)
2. Describe the working of a PN junction diode with neat diagrams. Also explain its V-I characteristics. (13 Marks) (May 2014), (May 2015) \& (Nov 2015) \& (April/May 2022) \& (April/May 2023) \& (Nov/Dec 2023)
3. Explain the operation of BJT in common emitter mode with its characteristics. (13 Marks) (Nov/Dec 2022)
4. Design a circuit to convert an voltage AC voltage into a DC voltage with a diode full wave bridge circuit and draw the resultant rectified waveform. (13 Marks) (April/May 2023)
5. Explain Bridge rectifier with suitable circuit diagram and derive its ripple factor ( $\mathbf{1 3}$ marks) (Nov/Dec 2022)
6. Explain Half wave rectifier with suitable circuit diagram and derive its efficiency, ripple factor, TUF and PIV. (13 Marks) (Nov 2015) \& (May 2016).
7. Describe the working of a zener diode with neat diagrams. Also explain its V-I characteristics. ( $\mathbf{1 3}$ Marks)
8. Explain with a neat sketch the construction and working characteristics of IGBT (OR) Explain the Constructional details and operation of IGBT (13 Marks) (Nov/Dec 2023)
9. Explain the Constructional details and operation of SCR ( $\mathbf{1 3}$ Marks)
10. Explain the mechanism of avalanche breakdown and zener breakdown.(8) (May 2016).
11. Explain the working of the CB configuration BJT. Draw its input and output characteristics. (13 Marks) (May 2014) \& (May 2015).
12. Explain the Constructional details and operation of JFET ( $\mathbf{1 3}$ Marks)

# UNIT - IV DIGITAL ELECTRONICS 

PART-A

1. Convert (634)s to binary. (May 2015) (Nov/Dec 2023)
$\begin{array}{lll}6 & 3\end{array}$
$110|011| 100$
$634)_{8}=(110011100)_{2}$.
2. Give the Truth table of XOR Gate. (Nov/Dec 2023)

TRUTH TABLE

| INPUTS |  | OUTPUT |
| :---: | :---: | :---: |
| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}=\mathbf{A B}{ }^{\prime}+\mathbf{A}^{\prime} \mathbf{B}$ |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ |

3. Calculated the number of bits affected if the data send speed is $\mathbf{1} \mathrm{Mbps}$ with the noise of $\mathbf{1} / 1000$ second. (April/May 2023)
Let's calculate the number of bits that will be affected using Shannon's theorem. $\mathrm{C}=\mathrm{B}$ $\log 2(1+$ SNR $)$
$\mathrm{C}=1000000 \log 2(1+1000) \mathrm{C}=1000000 \log 2(1001) \mathrm{C}=1,000,000 \times 9.967 \mathrm{C}=$ 9,967,000 bits per second

Therefore, the number of bits that will be affected if we are sending data at 1 Mbps with noise of- second. 1000 is $9,967,000$ bits per second.
4. Explain about SOP and POS form. (April/May 2023)

SOP represents Boolean terms as the sum of product terms. POS represents Boolean terms as a product of sum terms. SOP is more inclined towards minterms. POS favors maxterms.
5. What do you meant by weighted binary code? Give Examples (Nov/Dec 2022)

Weighted code: The code in which each and every bit position has a specified value or weight

Example: 8421, 5211 and 2421
6. What is meant by Combinational logic Circuit? Give Examples (Nov/Dec 2022)

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Combinational circuits are a kind of digital logic circuit whose instantaneous output depends only on the combination of its inputs. For example, a combinational circuit could be used to add any number of inputs, or to subtract them, or to perform other mathematical operations. In fact, one of the main applications of combinational circuits is to perform something called "Boolean Algebra," which refers to the performance of basic mathematical operations with binary numbers.

Combinational circuits are adder, Subtractor, multiplexer, Decoders, and Encoders.
7. Mention the significance of K-Map? (April/May 2022)

A K-map can be thought of as a special version of a truth table that makes it easier to map out parameter values and arrive at a simplified Boolean expression. A K-map is best suited for Functions with two to four variables.

K-map: Two variable map, Three variable map, Four variable Map.
8. Convert the given expression in canonical $S O P$ form $Y=A C+A B+B C$ ( $\mathbf{A} /$ May 2022)

$$
\begin{aligned}
\mathrm{Y} & =\mathrm{A}\left(\mathrm{~B}+\mathrm{B}^{\prime}\right) \mathrm{C}+\mathrm{AB}\left(\mathrm{C}+\mathrm{C}^{\prime}\right)+\left(\mathrm{A}+\mathrm{A}^{\prime}\right) \mathrm{BC} \\
& =\mathrm{ABC}+\mathrm{AB} \mathrm{~B}^{\prime} \mathrm{C}+\mathrm{ABC}+\mathrm{ABC}^{\prime}+\mathrm{ABC}+\mathrm{A}^{\prime} \mathrm{BC} \\
\mathrm{Y} & =\mathrm{ABC}+\mathrm{AB}^{\prime} \mathrm{C}+\mathrm{ABC}^{\prime}+\mathrm{A}^{\prime} \mathrm{BC} .
\end{aligned}
$$

9. Encode the word DATE in ASCII code.

ANS:D - 1000100 A - 1000001 T - 1010100 E - 1000101
10. Encode (1236) ${ }_{10}$ in Excess - 3 code

ANS (0101 01100111 1010) 2
11. Convert the following decimal numbers to octal (a) 79 (b) 0.925

ANS
(a) $8 \mid \underline{79}$

$$
8 \mid \underline{8-7} \underset{1-0}{ } \quad=(107)_{8}
$$

(b) $0.925 * 8=7.400$
$0.400 * 8=3.200$
$0.200 * 8=1.600$
$=(0.731)_{8}$
12. Convert the following Hexadecimal to Decimal (a) 4C5 (b) 0.9E8

ANS: (a) $=4 * 16^{2}+12 * 16^{1}+5 * 16^{0}$
$=(1217)_{10}$
(b) $=9 * 16^{-1}+14 * 16^{-2}+8 * 16^{-3}$
$=(1.18164)_{10}$
13. Perform the following Arithmetic operation

ANS: $\quad 1011.101$
$101.011{ }^{(-)}$
$\underline{110.010}$
14. What are non - weighted Code and Weighted Code?

Non weighted: The Code in which the bit position does not have any specified value.
Example: Excess-3 code, Gray code
Weighted code: The code in which each and every bit position has a specified value or weight
Example: 8421, 5211 and 2421
15. Convert (1259) 10 into Hexadecimal

ANS: $16 \underline{1259}$

$$
16 \mid 78-11
$$

$$
3-14
$$

$$
=(3 \mathrm{~EB})_{1}
$$

16. Convert (11101) gray to Binary code

ANS: Binary Equivalent $=(10110)_{2}$
17. What are the advantages of encoding a decimal number in BCD as compared with straight numbers?
The advantages of encoding a decimal number in BCD is that there is easier conversion between decimal and binary system .Moreover arithmetic operations are done in binary numbers in computers. Therefore encoding a decimal number in BCD is more advantageous.
18. What are Universal Gates? Why are they called so? What are their advantages? (

May 2015 ) $\boldsymbol{\&}($ Nov 2015)
Universal gates are NAND and NOR, they are called so because using these codes any logical gate or logical expression can be derived.
19. Add the decimals $57 \& 68$ using 8421 BCD code.

57+ $01010111+$
01101000
10111111
Add 6 to both $\underline{0110 \quad 0110}$
Groups $\underline{10010 \quad 0101}$
20. Convert $0.875_{10}$ to quandary (Base 5)

| $0.875 \times 5=4$ | +0.375 | $a_{-1}=4$ |
| :--- | :--- | :--- | :--- |
| $0.375 \times 5=1$ | +0.875 | $a_{-2}=1$ |
| $0.875 \times 5=4$ | +0.375 | $a_{-3}=4$ |
| $0.375 \times 5=1$ | +0.875 | $a_{-2}=1$ |

Answer: $0.875_{10}=\left(0 . \mathrm{a}_{-1} \mathrm{a}_{-2} \mathrm{a}_{-3} \mathrm{a}_{-4}\right)_{5}=(0.4141)_{5}$
21. Add the decimals $67 \boldsymbol{\&} 78$ using excess 3 code
$67+10011010$
$78 \quad \underline{10101011}$
101000101
22. Express the number (25) $)_{10}$ in Gray code.

| 2 | $\underline{25}$ |  |
| :--- | :--- | :--- |
| 2 | $\underline{12}$ | 1 |
| 2 | $\underline{6}$ | 0 |
| 2 | $\underline{3}$ | 0 |

1. 1

The equivalent binary is $(11001)_{2}$. Now the binary number (11001) is converted into Gray code.
(1): The LSB Gray digit is same as LSB binary
(2): Going from left to right add each adjacent pair of binary digit to get the next Gray code digit .
Discard carries. Therefore the corresponding Gray code for (11001) is 10101
23. What is register in digital system? (May 2016).

Registers are data storage devices that are more sophisticated than latches. A register is a group of binary cells suitable for holding binary information. A group of cascaded flip flop used to store related bits of information is known as register.

## 24. Describe the importance of EBCDIC code.

The extended Binary coded Decimal interchange code is an eight-bit code. This code is commonly used in Data transfer \& computer interface applications. In this case, the decimal digits are represented by the 8421 BCD code proceeded by 1111.

Since there is no carry, take 2 "s complement of resultant sum. Ans: -001010
25. State Demorgan's theorem: (May 2016).

Demorgan's theorem 1:

The complement of product of any number of variables is equivalent to sum of the individual complements.
Demorgan's theorem 2:
The complement of sum of any number of variables is equivalent to product of individual Complements.
26. Find the following binary difference: 1011010-0101110. (May 2013)

1011010
$\underline{0101110}$
$\underline{1010100}$

## PART-B \& C

1. Design and explain the working of Gray to BCD Converter. (9) (Nov/Dec 2023)
2. Convert $95.0625_{10}$ binary. (4) (Nov/Dec 2023)
3. Express the Function $\mathrm{Y}=\mathrm{A}+\mathrm{B}$ ' C in (13) (Nov/Dec 2023)
(i) Canonical SOP and
(ii) Canonical POS form
4. Explain different error detection technique and correction codes in detail. (13) (A/M 23)
5. Differentiate SOP and POS in digital Logic. (7) (A/M 23)
6. Minimize the expression
$\mathrm{Y}=\mathrm{AB}{ }^{\prime} \mathrm{C}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}+\mathrm{AB}^{\prime} \mathrm{C}^{2}+\mathrm{AB}^{\prime} \mathrm{C}^{\prime}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}^{\prime}$ using K Map (6) (A/M 2023)
7. Explain about the error detection and error correction codes (13) (N/D 22)
8. Simplify the Boolean function $\mathrm{f}(\mathrm{W}, \mathrm{X}, \mathrm{Y}, \mathrm{Z})=\mathrm{WX} \mathrm{X}^{\prime} \mathrm{Y}^{\prime}+\mathrm{WY}+\mathrm{W}^{\prime} \mathrm{YZ}$ ' using K-map. (13) (Nov/Dec 2022)
9. Design and explain the operation of full adder from its truth table (15) (Nov/Dec 2022)

(i) Design a Circuit using AND and OR gates to realize the above function (6)
(ii) Realize the above function using only NAND and NOR gates after simplification. (7)
10. For the truth table 1, obtain the simplified sum of products expression using K-Map realize using only NAND gates. Observe that this is the output of a majority voting circuit. (13) (April/May 2022)

## TRUTH TABLE 1

| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{C}$ | $\mathbf{Y}$ |
| :---: | :---: | :---: | :---: |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ |

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| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| :--- | :--- | :--- | :--- |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |

12. List various types of logic gates with its logic symbol and truth table. List also universal gates (13) (May 2016).
13. What is a combinational circuit? Explain the operation of Half and Full Adder circuit and Implement the sum and carry using NAND gate. (13) (May 2013)
14. Design a Full Adder, construct the truth table, simplify the output equations and draw the Logic Diagram. (13) (May 2016).
15. (i) Reduce the following expressions using Boolean algebra. (7) (May 2013)
$\mathrm{Y}=\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}^{\prime}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}+\mathrm{AB}^{\prime} \mathrm{C}^{\prime}+\mathrm{ABC}$.
$\mathrm{Y}=\left[(\mathrm{A}+\mathrm{B})^{\prime}+\mathrm{C}^{\prime}\right]^{\prime}$.
(ii) Realize the given expression using only NAND gates and Inverters. (6) (May2013)

$$
\mathrm{Y}=\mathrm{ABC}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}^{\prime} .
$$

